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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,563	11/13/2003	Robert M. Ellis	5038-298	8266
32231 7590 09/27/2007 MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204			EXAMINER KROFCHECK, MICHAEL C	
			ART UNIT 2186	PAPER NUMBER
			MAIL DATE 09/27/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/713,563	Applicant(s) ELLIS, ROBERT M.	
	Examiner Michael Krofcheck	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 July 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17 and 22-26 is/are pending in the application.
- 4a) Of the above claim(s) 16, 17 and 22-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15, 25 and 26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some    \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

1. This office action is in response to the amendment filed on 7/25/2007.
2. Claim 27 has been cancelled.
3. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
6. Claims 1-7, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al., US patent application publication 2002/0112119, and Bashirullah et al., US patent application publication 2005/0005046.

Art Unit: 2186

7. With respect to claim 1, Halbert teaches of a point-to-point memory channel having a plurality of data lanes (fig. 10-13; paragraph 0053-0056; Shown in figures 10 and 12, the paths contain multiple lanes).

Halbert fails to explicitly teach of calculating an achieved data transition density for at least one data lane, the achieved data transition density calculated over greater than two clock cycles; and transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density.

However, Bashirullah teaches of calculating an achieved data transition density for at least one data lane, the achieved data transition density calculated over greater than two clock cycles (paragraph 60, 78);

transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density (paragraph 58-60).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, and Bashirullah at the time of the invention to include the adaptive bandwidth bus of Bashirullah in communicating to the memory of Halbert. Their motivation would have been to reduce the power dissipation (Bashirullah, paragraph 46).

8. With respect to claim 2, Bashirullah teaches of wherein calculating an achieved data transition density for the at least one data lane comprises: counting how many times a data transition occurs on the at least one data lane during a predetermined number of clock cycles, the predetermined number of clock cycles being greater than two (paragraph 60, 78).

9. With respect to claim 3, Bashirullah teaches of storing a desired data transition density for the at least one data lane; and comparing the achieved data transition density to the desired data transition density (paragraph 60, 78; as the threshold is set a 1, it must be kept track of somewhere and compared to the occurred transitions).

10. With respect to claim 4, Bashirullah teaches of wherein transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density comprises: transmitting a synchronization signal on all the data lanes if the achieved data transition density is less then the desired data transition density on the at least one data lane (paragraph 58-60).

11. With respect to claim 25, Bashirullah teaches of wherein transmitting the synchronization signal on the at least one data lane comprises: transmitting the synchronization signal having a number of transitions to cause the achieved data transition density for the at least one data lane is greater than or equal to a desired data transition density (paragraph 58-60).

12. With respect to claim 5, Halbert teaches of a memory channel comprising: a host and a plurality of DIMMs connected in a point-to-point fashion (fig. 10-13; paragraph 0054-0055),

wherein the host includes a processor (paragraph 0004);

an outbound data channel and an inbound data channel, each having a plurality of data lanes (fig. 10-13; paragraphs 0053-0056, 0058; where an embodiment can be constructed using two data paths (channels) with unidirectional components; thus

Art Unit: 2186

creating an outbound and an inbound path. Shown in figures 10 and 12, the paths contain multiple lanes);

Bashirullah teaches of at least one transition detection circuit configured to detect whether an achieved data transition density on at least one data lane is less than a desired data transition density for the at least one data lane (fig. 4; 58-61).

wherein the achieved transition density is measured over greater than two clock cycles (paragraph 78; where  $C_p$  is 3 clock cycles).

13. With respect to claim 6, Bashirullah teaches of wherein the at least one transition detection circuit is located on the host (paragraph 46-47; the adaptive bandwidth bus is inter-chip or off chip).

14. With respect to claim 7, the combination of Halbert and Bashirullah teaches of the at least one transition detection circuit is located on a corresponding one of the plurality of DIMMs (Halbert, fig. 10-13; paragraph 58; Bashirullah paragraph 46-47; in the unidirectional path of Halbert transmitting from the memory, the adaptive bandwidth bus must also be originating in the DIMM to impart the bandwidth changing of Bashirullah in that direction).

15. With respect to claim 26, the combination of Halbert and Bashirullah teaches of the transition detection circuit is configured to detect whether an achieved data transition density on a corresponding one of the at least one data lane is less than the desired data transition density for the corresponding data lane (Bashirullah, fig. 4; paragraph 58-60).

16. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert and Bashirullah as applied to claim 5 above, and further in view of Boggs, et al., US patent 5530696.

17. With respect to claim 8, Bashirullah teaches of wherein the at least one transition detection circuit comprises: a plurality of data transition detectors, each configured to detect a data transition on a corresponding data lane (fig. 4; paragraph 57);

a clock cycle counter (paragraph 60; as a predetermined number ( $C_p$ ) of clock cycles are kept track of, there must be a clock cycle counter);

The combination of Halbert and Bashirullah fails to explicitly teach of a plurality of data transition counters, each configured to count the data transitions, and configured to be reset by the clock cycle counter.

a plurality of data transition counters, each configured to count the data transitions, and configured to be reset by the clock cycle counter (fig. 2; column 6, lines 22-32, 41-46);

The combination of Halbert, Bashirullah and Boggs teaches of a logic block configured to signal when at least one of the plurality of data transition counters counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density (Bashirullah, fig. 4; paragraph 58-60).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Bashirullah and Boggs at the time of the invention to include the counters of Boggs in the combination of Halbert, and Bashirullah. Their motivation would have

been to provide increased flexibility in the driver in the combination of Halbert and Bashirullah, which also allows for monitoring of transitions on a longer scale for better overall efficiency.

18. With respect to claim 9, Boggs teaches of wherein the clock cycle counter and the plurality of data transition counters are programmable (fig. 2; column 5, lines 51-61; column 6, lines 15-32; as the counter (clock cycle counter) and the asynchronous counter (transition counter) are integrated circuits, it is abundantly clear to one of ordinary skill in the art that they are programmable).

19. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, Bashirullah and Boggs as applied to claim 8 above, and further in view of the applicant's admitted prior art (AAPA).

20. With respect to claim 10, Halbert, Bashirullah and Boggs fails to explicitly teach of wherein the logic block comprises an AND gate and a plurality of NAND gates.

However, AAPA teaches of wherein the logic block comprises an AND gate and a plurality of NAND gates (specification page 4, lines 18-21, 25-27).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Bashirullah, Boggs and AAPA at the time of the invention to include the NAND and AND gates of AAPA in the combination of Halbert, Bashirullah, Boggs. Their motivation would have been to as those with ordinary skill in the art are familiar with using the NAND and AND gates to create output signals (AAPA, page 4, lines 19-21, 25-27) such as the control signal of Bashirullah.



21. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert and Bashirullah as applied to claim 5 above, and further in view of Boggs.

22. With respect to claim 11, the combination of Halbert, Bashirullah, Boggs teaches of the limitations cited with respect to claim 8. Additionally, the combination teaches of the above first logic block with respect to data lanes on the outbound data path (Halbert, fig. 10-13; paragraphs 0053-0056, 0058; as the unidirectional components create an inbound and outbound path. Bashirullah, paragraph 46-47 as mentioned with respect to claim 7).

The combination of Halbert, Bashirullah, and Boggs, teaches of a second logic block analogous to the first logic block taught above, but is located in the CPU of Halbert on the output of the CPU, thus on the inbound data lines of the memory (Bashirullah, paragraph 46-47).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Kim, Wong, Boggs at the time of the invention to include a data output driver of Kim in the CPU of Halbert, which is supported by Little. Their motivation would have been to reduce the skew of the output of data (Kim, paragraph 0009).

23. With respect to claim 12, Boggs teaches of the limitations as cited with respect to claim 9.

24. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, Bashirullah, Boggs as applied to claim 11 above, and further in view of AAPA.

25. With respect to claim 13, AAPA teaches of the limitations as cited above with respect to claim 10.

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Bashirullah, Boggs, and AAPA at the time of the invention to include the NAND and AND gates of AAPA in the combination of Halbert, Bashirullah, Boggs. Their motivation would have been to as those with ordinary skill in the art are familiar with using the NAND and AND gates to create output signals (AAPA, page 4, lines 19-21, 25-27) such as the control signal of Bashirullah.

26. Claims 14-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert, Bashirullah, Boggs, and Bliss et al., US patent application publication 2004/0056782.

27. With respect to claim 14, Halbert teaches of a data lane in a point-to-point memory channel (fig. 10-13; paragraph 0053-0056);

Bashirullah teaches of storing a desired data transition number (paragraph 58-60; it is abundantly clear to one of ordinary skill in the art that the threshold number is has been stored since it is needed);

recording a measured data transition number (paragraph 58-60; it is abundantly clear to one of ordinary skill in the art that the transition number has been stored);

comparing the measured data transition number to the desired data transition number (paragraph 58-60)

storing a clock cycle number (paragraph 60; as the clock cycle number is predetermined it must be stored);

Boggs teaches of recording a measured data transition number over a period of clock cycles equal to the clock cycle number (fig. 2; column 6, lines 22-32, 41-46);

Bashirullah teaches of the clock cycle number being greater than two (paragraph 78).

The combination of Halbert, Bashirullah, and Boggs fails to explicitly teach of a machine-readable medium, that when read, causes a machine to perform processes. However, Bliss teaches of a machine-readable medium, that when read, causes a machine to perform processes (paragraph 0017).

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Bashirullah and Boggs at the time of the invention to include the counters of Boggs in the combination of Halbert, and Bashirullah. Their motivation would have been to provide increased flexibility in the driver in the combination of Halbert and Bashirullah, which also allows for monitoring of transitions on a longer scale for better efficiency.

It would have been obvious to one of ordinary skill in the art having the teachings of Halbert, Bashirullah, Boggs, and Bliss at the time of the invention to incorporate the processes and software carrying out the combination of Halbert, Bashirullah, and Boggs into the computer readable medium of Bliss. Their motivation would have been to provide for ease of upgrading and portability.

28. With respect to claim 15, Bashirullah teaches of transmitting a synchronization signal on the data lane if the measured data transition number is less than the desired data transition number (cited above with respect to claims 1 and 5).

***Response to Arguments***

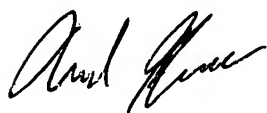
29. Applicant's arguments, see 8/7/2007 interview summary and applicant's remarks page 8, third bullet, filed 7/25/2007, with respect to the rejection(s) of claim(s) 1-5, 7, and 25 under Halbert, Kim, and Wong have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bashirullah.

***Conclusion***

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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